WHAT IS CLAIMED IS:

1. An integrated circuit semiconductor device, comprising:

a semiconductor substrate;

one or more metallurgy layers connected to the semiconductor substrate, wherein each of the one or more metallurgy layers comprises one or more conductive lines and one or more dummy structures between the one or more conductive lines wherein at least two of the one or more dummy structures from different metallurgy layers are thermally connected; and

one or more dielectric layers between the one or more metallurgy layers.

2. The semiconductor device of claim 1 wherein at least two of the one or more dummy structures on a first metallurgy layer are connected to at least two of the one or more dummy structures on a second metallurgy layer through a plurality of vias.

3. The semiconductor device of claim 1 wherein at least one of the one or more dummy structures comprises copper.

4. The semiconductor device of claim 1 wherein at least one of the one or more dummy structures comprises aluminum.

5. The semiconductor device of claim 1 wherein the distance between one of the dummy structures and one of the one or more conductive lines is at least 0.1um.

6. The semiconductor device of claim 1 wherein the width of one of the one or more dummy structures is substantially the same as the width of one of the one or more conductive lines.

7. The semiconductor device of claim 1 wherein the two dummy structures comprise different shapes.

8. The semiconductor device of claim 1 wherein the two dummy structures comprise different materials.

9. The semiconductor device of claim 1 wherein the two dummy structures comprise different sizes.

10. The semiconductor device of claim 1 wherein the two dummy structures are connected by a first line, wherein the width of the first line is less than the width of each of the two dummy structures.

11. The semiconductor device of claim 10 wherein the first line comprises copper.

12. The semiconductor device of claim 10 wherein the first line comprises aluminum.

13. The semiconductor device of claim 12 wherein another two dummy structures are connected by a second line, wherein the first line and the second line comprise identical materials.

14. The semiconductor device of claim 12 wherein the first line and the second line comprise different materials.

15. A method of fabricating a semiconductor device that provides heat dissipation, comprising:

providing a first metallurgy layer wherein the first metallurgy layer includes a plurality of conductive lines and one or more areas between the conductive lines;

supplying one or more dummy metal structures in the one or more areas; and

connecting at least two of the one or more dummy metal structures to dissipate heat.

16. The method of claim 15 further comprising providing a plurality of dummy metal structures to one or more other metallurgy layers of the semiconductor device wherein the plurality of dummy metal structures of the other metallurgy layers are connected to the one or more dummy metal structures of the first metallurgy layer through a plurality of vias.

17. The method of claim 15 wherein the dummy metal structures are uniformly spaced.

18. The method of claim 15 wherein the dummy metal structures are non-uniformly spaced.

19. An integrated circuit semiconductor device, comprising:

a semiconductor substrate;

one or more metallurgy layers connected to the semiconductor substrate, wherein each of the one or more metallurgy layers comprises:

one or more conductive lines;

one or more dummy metal structures between the one or more conductive lines wherein at least two of the one or more dummy metal structures are connected by metal lines, wherein the distance between each of the dummy metal structures and each of the conductive lines is at least 0.1um; and

one or more dielectric layers between the one or more metallurgy layers, wherein the one or more dummy metal structures on a first metallurgy layer are connected to the one or more dummy metal structure on a second metallurgy layer through vias.

20. The integrated circuit semiconductor device of claim 19 wherein the respective heights of the metal lines and the dummy metal structures are similar.